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Digital Generation and Phasing of Transmitter Signals for SuperDARN Class Radars

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Abstract

It is planned that the TIGER N.Z. radar will be a digital evolution of the current analog system, where the phasing matrix for both transmitter and receiver arrays, and the receiver architecture will be implemented in Field Programmable Gate Array (FPGA) technology. Producing a fully digital system in FPGA technology allows a different solution to the current analog approach. An added challenge is the utilization of the DSP techniques such as multirate filters to enhance the performance of the implementation. In this paper we discuss our proposal for a digital SuperDARN radar. Our initial investigations are presented, which we believe not only demonstrate that the concept is feasible, but that a digital radar will provide many benefits to the SuperDARN community.

Introduction - DSP and software radio

Digital signal processing (DSP) has become an integral part of wireless communication systems. Increasingly, traditional analog sections of transmitter and receiver circuits are being replaced by more efficient DSP solutions. Not only are DSP solutions well placed to take every advantage of the rapid advances in Integrated Circuit technology, but we can also employ DSP techniques in ways that have no direct analog counter part [1]. Gorden Moore's law suggests that every 18 months the IC gate count doubles and the operating frequency increases by 50%. It is highly likely that Moore's law will hold over the coming decade. Paraphrasing Moore's law we see that, the cost of performing a waveform processing task using DSP halves every eighteen months, decreases by an order of magnitude every four years, and becomes roughly 30% faster each year.

The advantages of digitization and the advances forecast by Moore's law can be seen in the increasingly enhanced features and flexibility of many consumer products today. The best example is probably the mobile phone, where core functions are now entirely digital, DSP techniques are used extensively throughout the design, and new products appear almost weekly.

Most high volume electronic products, such as mobile phones, are implemented using Application Specific Integrated Circuits (ASICs). In an ASIC the required electronic design is imprinted directly onto the silicon. The result is a relatively low unit cost for high volume production. However, as the cost for the initial set up of an integrated circuit fabrication run can run to several million dollars, this is not an option for low volume production. An alternative is the Field Programmable Gate Array (FPGA). A FPGA is an integrated circuit

that contains a sea of generic components, which can be configured and connected to one another in enormous variety of different ways. In most FPGAs the configuration and connection information is stored in static RAM. This type of FPGA can be re-programmed with a new design in a matter of seconds. A fast design turn around time makes FPGAs ideal for prototyping. FPGAs can also be used to produce reconfigurable hardware - where the same piece of hardware performs different functions at different times (by simply re-programming it's on board FPGA(s)).

While FPGAs are roughly an order of magnitude behind ASICs in performance. The good news is that Moore's law also applies to FPGAs, and FPGA vendors have recognised the potential of digital signal processing and are now producing FPGAs tailored to DSP solutions [2]. Recent advances in Field Programmable Gate Array technology mean that complex DSP systems can now be incorporated into one easily re-configurable device, providing an invaluable tool for the development of prototype and small production scale digital radio systems [3].

Current Analog System

The current analog TIGER system is based on the University of Leicester implementation, which builds on the work of the other radar groups most notably the original radar from the Applied Physics Laboratory at Johns Hopkins University. The TIGER transmitter is set of 16 transmitters connected to a log-periodic antenna array and with a frequency range varying from 8MHz to 20 MHz. This operating frequency enables the transmitted vector to achieve oblique incidence in the ionosphere and reflect back to the radar receiver [4]. Each beam is transmitted at 600W and is directed through a phasing matrix, which adds the appropriate delay to each transmitted signal to steer the beam. The block diagram of the TIGER radar is shown in Figure 1, which outlines mainly the transmitter section.

The analog frequency synthesizer has main role in selecting the operational frequency for the transmitter beam. The mixing operation is performed using a local oscillator with frequency range of 48-60 MHz and multiplied with a reference input of 40.625 MHz. A bandpass filter is used to suppress frequencies out of 8-20 MHz bandwidth. The timing pulses are controlled by a computer and are normally not continuous. A regular pulse train for the radar is not suitable because of Doppler shift in the echoes; therefore pulse train with varying time slots is modulated. The typical pulse length is 300usec for 45Km range resolution and radar uses a number of different multipulse transmission sequences consisting of typically 13 pulses over a100ms time frame [5].

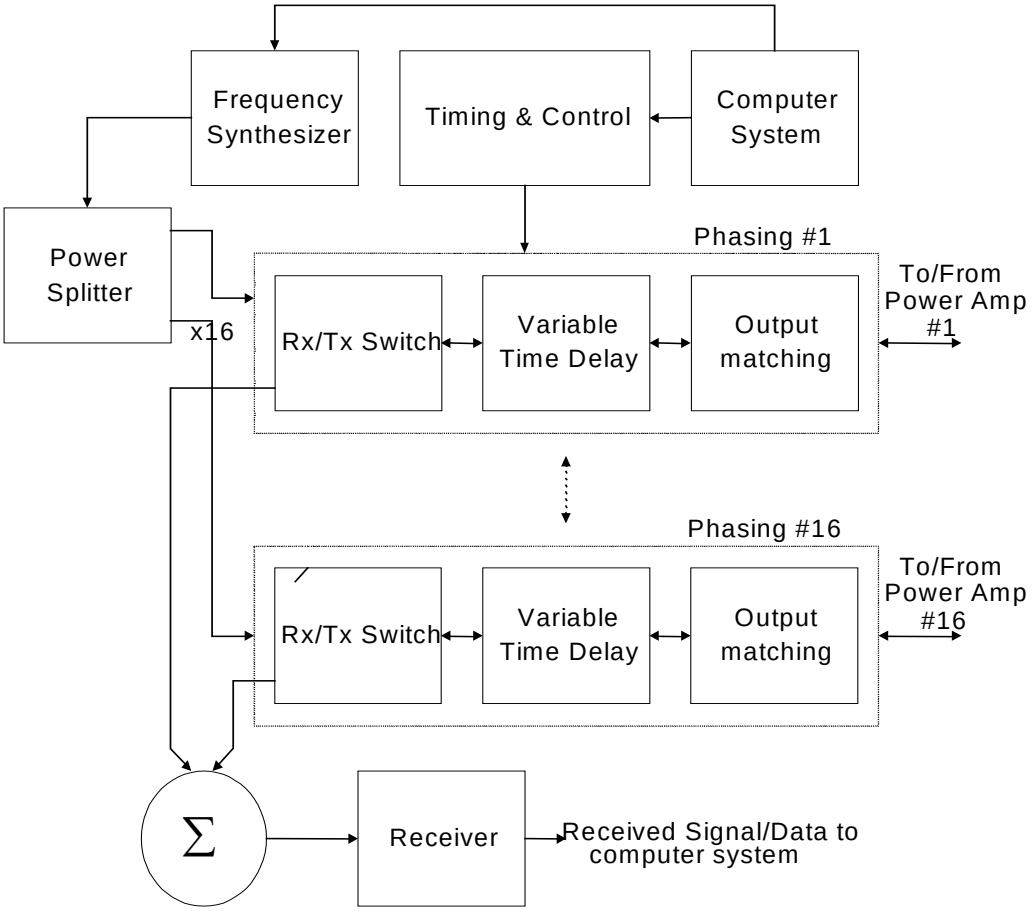


Figure 1, Simplified Block Diagram of TIGER Radar

The transmitted beams are centered at intervals of approximately 3.6 degrees and 16 beams give azimuth sweep of approximately 52 degrees. The bi-directional phasing matrix is implemented as a switched variable time delay, with fixed settings for each of the 16 beams. This means the phase delay varies with frequency. The azimuth beam width also decreases with an increase in frequency [5].

Digital Tiger - Why go digital?

It is planned that the TIGER N.Z. radar will be a digital evolution of the current analog system, where the phasing matrix for both transmitter and receiver arrays, and the receiver architecture will be implemented in FPGA technology. Producing a fully digital system in FPGA technology allows a different solution to the current analog approach. The digital system will be easier to build with little, if any, tuning and set-up required which will save time and effort in construction and, importantly, the ongoing maintenance of the system. The digital system also integrates many large function blocks (e.g. the synthesizer) into smaller gate arrays, which will significantly reduce the size of the system. For example, we propose to reduce the left-hand equipment rack of the current TIGER system (see figure 2) to three modules with a total height of less than 6" (150cm) - as shown in figure 3.

With the advances in microelectronics in recent years, communications systems have migrating more and more functions to digital implementations. We are able to leverage

existing digital radio techniques and microelectronic advances, and adapt them to our needs, as well as adding our own innovations. In addition to these benefits, an implementation in FPGA technology will allow reconfiguration of the system on the fly to enable different features or system configurations to be switched in or out in less than a minute.

Figure 2, Current TIGER Equipment Racks

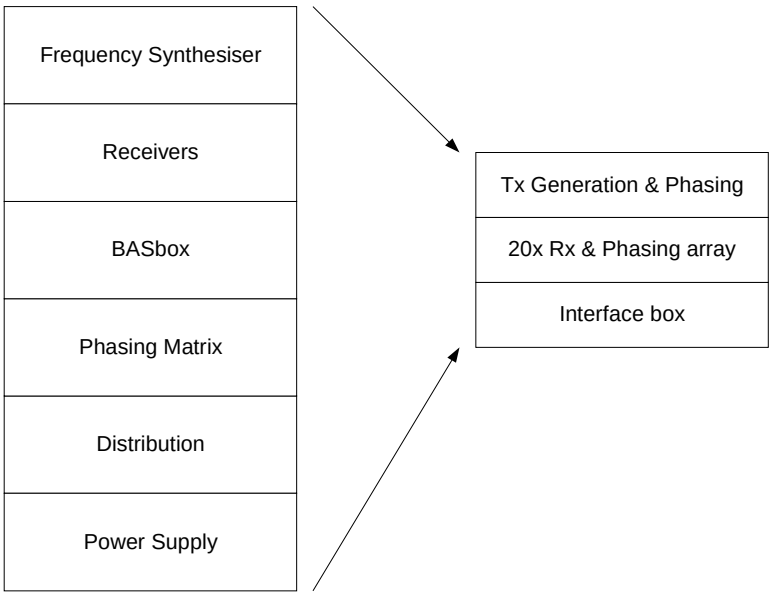


Figure 3, Proposed Reduction of Left Hand Rack

In summary, a fully digital TIGER radar would feature:

- a digital frequency Synthesizer - providing greater control over transmission frequencies and a higher quality signal;

- a digital phasing matrix - while the digital version will require two phasing blocks (for transmit and receive), the quality and flexibility of phasing will be far superior to the current system;

- a true gaussian pulse - this will greatly reduce any interference caused by side lobes; this is of particular importance for the TIGER radar, as the Australian Communications Authority has expressed it's displeasure over the additional 70kHz lobes existing in the analog system (70kHz from the noise floor not the 3dB point);

- fully digital control signal distribution (BASbox);

- a digital system interface via parallel I/O ports - while this would streamline operations in the long run and allow for the inclusion of some additional features, it would require new software, a new QNX driver and possible modifications to the Radops code; thus in the initial implementation the digital receiver output will be converted to an analog signal, and then resampled by AtoD converters in timing computer as per the existing system.

Proposed Digital System

RF modulation can be achieved using techniques that involve sine or cosine multiplication of power sensitive signals. Using multirate DSP techniques this can be implemented in relatively straightforward digital logic. Here we propose an equivalent digital method of generating transmitter signals for existing analog TIGER SuperDARN radar. Our proposed digital system replaces the beam generation system of the transmitter, with power amplifier and other associated analog circuitry remaining the same. A block diagram of the proposed method is shown in Fig. 4.

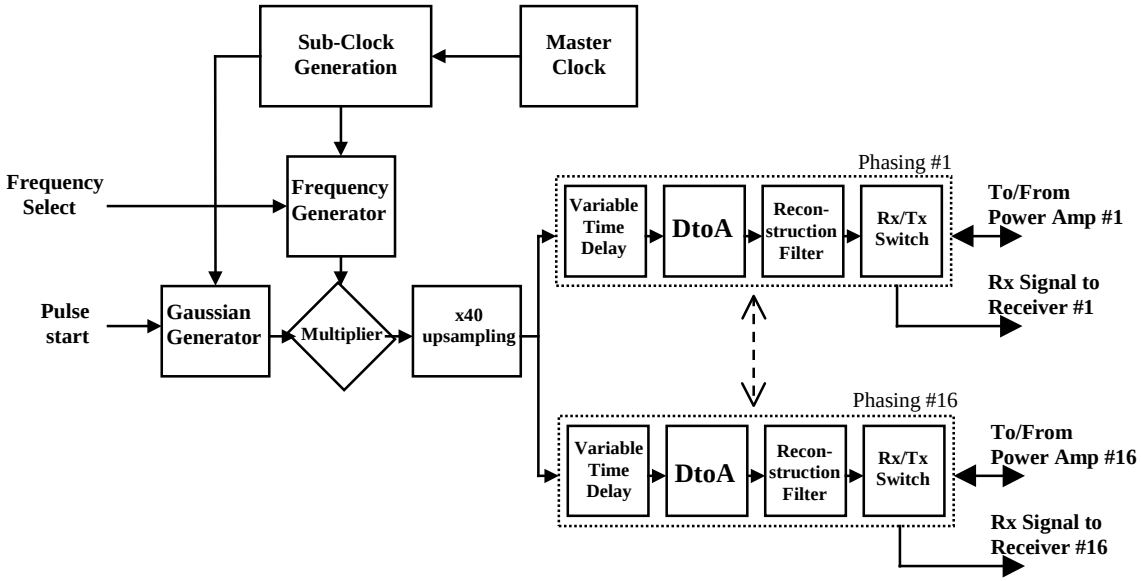


Figure 4, Proposed TIGER Digital Transmitter - Block Diagram

The proposed digital transmitter consists of eight major elements: master clock and sub clock generation; gaussian generator; frequency generator; multiplier; upsampler; phasing matrix;

digital to analog conversion (DtoA); and the reconstruction filter. Each of these is discussed in turn.

Master clock and sub clock generation - high-speed system clock (in the order of 200 to 400 MHz) with low phase noise will be required to meet the specifications outlined below. At these frequencies clock skew, clock jitter, and clock distribution become significant issues. While the latest FPGA devices have been designed to minimize clock skew and clock distribution problems, where possible, it is advantageous to run sub systems at lower clock rates.

The gaussian generator - this consists of a look up table, in which the values of a sampled gaussian pulse are stored (in read only memory (ROM)), and index circuitry. As a gaussian pulse is symmetrical with many samples at zero (at either ends of the pulse), only half the non-zero sample values need be stored. This method provides considerable savings on the memory space required with only a small increase in the complexity of the index circuitry. The number of samples and the clock rate sets duration of the gaussian pulse (in this case 290μs). The current analog analog system uses pseudo gaussian shaping circuit (RC shaping at the final transmitter amplifier). In the digital implementation the accuracy of the gaussian pulse is only limited by the number of bits used to represent the wave shape.

Frequency generator - a DSP sine wave generator, equivalent to the analog frequency synthesizer. This section generates the carrier frequency (before upsampling) for the transmitted signal. Major issues here are frequency resolution and phase error, or jitter, which determines the spectral width of the output frequency. We are aiming for an output (after upsampling) resolution of 100Hz or better, and a phase error $< 10^{-9}$.

Multiplier - convolves the gaussian pulse with the local oscillator signal to produce a modulated gaussian signal. A digital signed multiplier is used with the number of bits dependant on the output requirements (DtoA), plus a few additional bits to minimize fixed point arithmetic (truncation/rounding) errors in the following stages.

Upsampler - a resample of the input signal at a higher clock rate followed by a digital filter that selects the wanted frequency band (in this case 8-20MHz). Upsampling is a multirate DSP technique that provides a relatively simple method of frequency shifting. An added bonus is that it allows for lower frequencies and clock rates to be used in parts of the system (in this case the gaussian generator, frequency generator and multiplier), resulting in circuitry savings.

Phasing matrix - introduces the required phase delays to the sixteen antennas, thus steering the beam. We must generate phasing for 16 beams, over 52 degrees of azimuth, at 3 – 4 degree steps per beam. One option for implementation would be to use 16 parallel delay registers. However, at a maximum frequency of 20MHz, we have 50ns/360 seconds/degree, that gives less than 1ns per degree. Thus, we would require a clock in the order of 10GHz and very large delay registers. This solution would be very expensive in real estate and a 10GHz clock is not possible even in present ASIC technology. A more realistic implementation is to use a poly-phase filter (or transform as suggested by fred harris). An interesting characteristic of this time-variant technique, a DSP structure that has no analog equivalent, is that phasing and upsampling (frequency shifting) can be done in one step. The phasing matrix in the digital transmitter will be uni-directional and thus a separate phasing matrix will be required for the receiver.

Digital to Analog conversion - requires high-speed conversion at greater than 100MHz. The noise floor is set by quantization noise of the DtoA, which is dependent on the number of bits used in the conversion. The current analog system has a worst case noise floor of 72dB, with spurii and harmonics of the fundamental signal at only 36dB (worst case). Our aim would be to achieve a noise floor of greater than 80dB. 13bits should provide this figure (6dB per bit + 3dB), however, DtoA converters are usually only available in even numbers of bits. 14bits would be a good choice, the additional accuracy would also account for any linearity issues, although 12bits could be used for have equivalent performance to current analog system.

Reconstruction filter - (Analog) to achieve the nyquist criterion with a reasonable filter size we have set the sample rate to be 10 times the niquest frequency (40MHz) for our maximum signal frequency (20MHz), giving a sample rate of 400MHz. A 5 pole filter will provide 100dB/decade roll-off, although practicalities of the system mean that the power amplifier will not amplify above 30MHz. Thus, a lower clock rate could be used with the power amplifier included as part of the filter function. Hence, a 100 - 200MHz output sample rate may be achievable with no reduction of signal quality. A higher order filter could also be used to lower the clock rate. Although, the system will be very sensitive to differential phase changes through the 16 filters - thus the simpler we can make analog filter stage the better!

Work undertaken to prove concept

At present our investigations to prove the digital TIGER concept have consisted of the following two strategies. (a) The implementation in FPGA hardware of scaled down version of a number of the elements discussed in the previous section and (b) the modeling of potential DSP structures in Matlab.

Hardware implementation

We have successfully implemented a scaled version of the gaussian modulation circuit in an FPGA device. The circuit, shown in the block diagram below (figure 5), consists of a gaussian generator, frequency generator and multiplier block. This represents the proposed circuitry before unsampling and phasing.

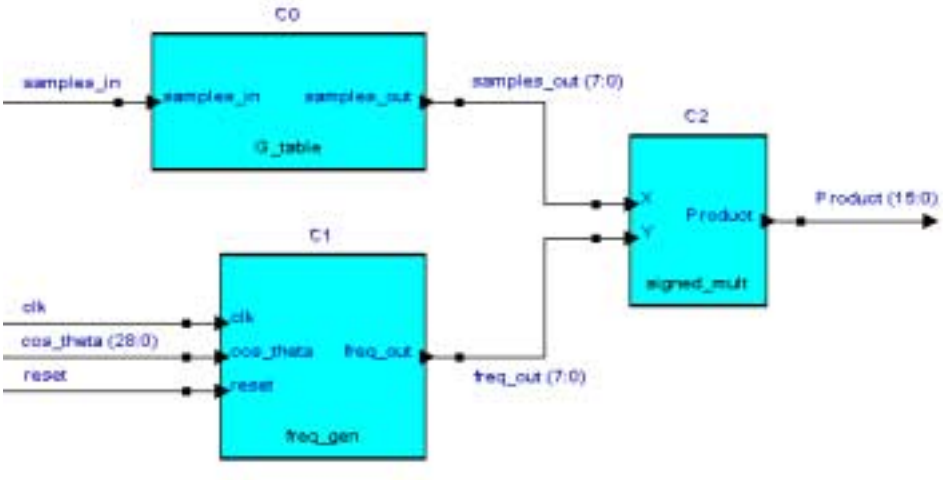


Figure 5, Gaussian Pulse Modulator - Block Diagram

The output of the scaled version was connected to a readily available 8bit Digital to Analog (DtoA) converter. As the available DtoA was only designed for audio frequency type applications the maximum output frequency and sample rate were scaled down by a factor of 1000. That is a maximum carrier frequency of 500Hz, equivalent to 20MHz (500 x 1000 x 40 (upsampling)), and a sampling frequency of 20kHz, equivalent to 400MHz (20000 x 1000 x 40). As the DtoA for this investigation was limited to 8bits, this restriction was placed on the outputs of the gaussian generator and the frequency generator. Also, only the most significant 8 bits of the multiplier output were connected to the DtoA.

The Gaussian generator consists of a simple 50 sample x 8bit look-up table with a revolving index incremented after each sample and reset when the maximum index is reached. The multiplier consists of a signed 8x8bit parallel array multiplier. While both these structures faithfully represent scaled operational functionality of the proposed elements in the digital transmitter, their architecture is not representative of a likely final version. In the full-scale implementation special FPGA architectural features, such as embedded memory and multiplier circuits, will be utilized to provide a faster and more efficient implementation.

The frequency generator is an important part of the proposed digital transmitter. For the characteristics of the transmitter signals depend significantly on the quality of the frequency generator output. With this in mind a considerable investigation was undertaken to analyze and quantify an appropriate architecture for this purpose. The frequency generator is based on a single multiplier sine-cosine generator described by Mitra [6] and shown in figure 6 below.

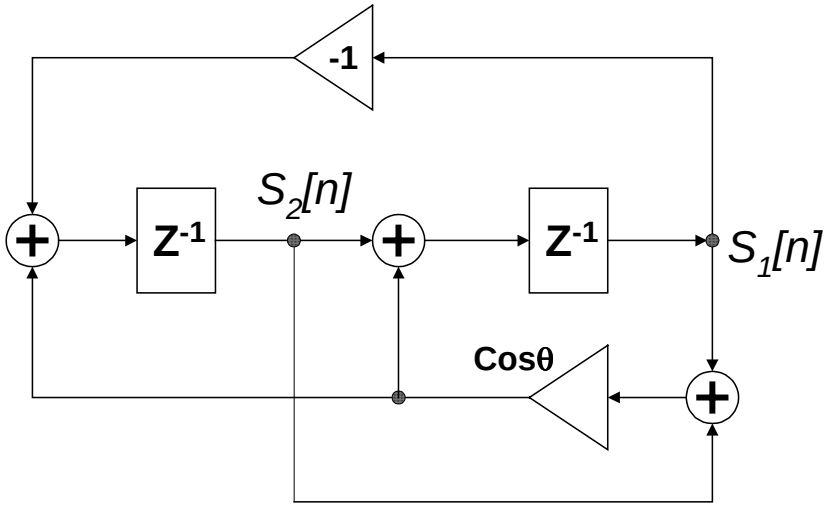
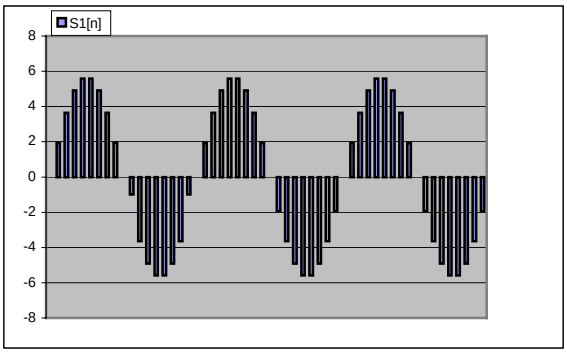


Figure 6, Single Multiplier Sine-Cosine Generator

In this circuit the multiplication factor Cosθ and the sample rate determine the output frequency. Both sine (S_1) and cosine (S_2) outputs are available. However, while the cosine output always has a magnitude of one (1), the magnitude of the sine output varies depending on the value of θ (but is always greater than 1). A sample of the output values over time is shown in figure 7. In this example Cosθ = 0.94 ($\theta = 20^o$) and the peak amplitude of the sine waveform (S_1) is 5.67.



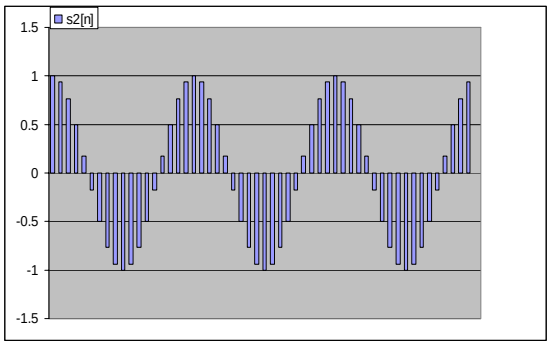


Figure 7(a), Sample Sine Output S_1 Figure 7(b), Sample Cosine Output S_2

Clearly, the cosine output, due to its fixed magnitude, is the most appropriate for our application. Although the magnitude of the sine output must be factored into the design as this signal is feedback and used in the calculation of future output values. While the operation of this circuit can be easily modeled using floating point arithmetic, as in the above example, an efficient hardware implementation must use fixed-point arithmetic. In circuits such as this, choosing the correct number of bits is an important part of the design process. If too few bits are used, arithmetic errors will become significant and result in poor quality of output. On the other hand if too many bits are used then precious hardware space and possibly speed will be wasted. In this circuit both the fraction portion (required to accommodate Cosθ) and the integer portion (required to maintain peak amplitude of the sine output) must be considered.

Frequency Generator - Analysis

Firstly, we shall investigate the output frequency, how it is derived, and the number of bits required for its calculation. The output frequency (f) is dependant on the Cosθ input and the sample clock rate (clk).

$$f = \frac{clk \cdot \theta}{360}$$

From this, we see that as

$$Cos\theta \to 1, \theta \to 0 \; and \; f \to 0$$

Now the peak amplitude of the Sine output has been calculated to be

$$Peak\_Amp = \frac{Cos\theta + 1}{Sin\theta}$$

and so, as

$$Cos\theta \to 1, Sin\theta \to 0 \; and \; Peak\_Amp \to \infty$$

Thus, the peak amplitude in a particular implementation is set by the minimum output frequency (f_{min}), and the clock rate.

$$Peak\_Amp = \frac{Cos\left(\frac{360 \cdot f\min}{clk}\right)+1}{Sin\left(\frac{360 \cdot f\min}{clk}\right)}$$

Which in turn sets the number of integer bits required for the fix point arithmetic internal to the frequency generator.

The second issue of importance in our analysis is the output frequency resolution (Δf) and the required number of fraction bits. As shown in figure 8, the lower the output frequency (f) the greater the resultant change in Δθ (and hence Δf) for a fixed change in Cosθ (ΔCosθ).

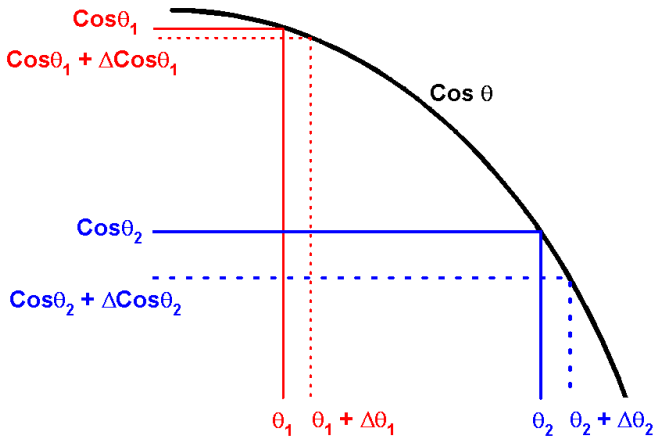


Figure 8, Cosθ Resolution

Thus, the resolution of Cosθ (ΔCosθ) is not only set by the required output frequency resolution (Δf), but also, the minimum frequency (f_{min}) and the clock rate (clk). Hence, the require fraction bits can be calculated from the following formula.

$$Cos\theta\_bits = \log_2\left[\frac{1}{Cos\left(\frac{f\min \cdot 360}{clk}\right) - Cos\left(\frac{(f\min + \Delta f)\cdot 360}{clk}\right)}\right]$$

Frequency Generator Design

An inspection of the previous formulae reveals that the ratio f (or f_{min}) to clk is common throughout. This has enabled us to design a frequency generator circuit to meet the required specifications of the final digital transmitter, and by simply scaling back the sample rate (clk) its operation can be matched to that of the other elements in the proof of concept implementation.

Frequency Generator – Design Specifications:

- Frequency range: 200kHz – 500kHz (8 – 20MHz after x40 upsampling);
- Frequency resolution of 2.5Hz (100Hz after x40 upsampling)
- Sample rate (clk) = 10MHz, gives a sample rate of 400MHz after x40 upsampling (set by requirement of the reconstruction filter)
- Phase error < 10-9, in this implementation the phase error of the output frequency is determined by the phase noise of the master clock.

Using these specifications the required fixed-point arithmetic bits were calculated.

$$Peak\_Amp = \frac{Cos\left(\frac{360 \cdot f_{\min}}{clk}\right)+1}{Sin\left(\frac{360 \cdot f_{\min}}{clk}\right)} = \frac{Cos\left(\frac{360 \cdot 0.2}{10}\right)+1}{Sin\left(\frac{360 \cdot 0.2}{10}\right)} = 15.9$$

Thus, to represent a peak amplitude of 15.9 we require 5 integer bits.

$$Cos\theta\_bits = \log_2\left[\frac{1}{Cos\left(\frac{f_{\min} \cdot 360}{clk}\right) - Cos\left(\frac{(f_{\min}+\Delta f)\cdot 360}{clk}\right)}\right]$$

$$Cos\theta\_bits = \log_2\left[\frac{1}{Cos\left(\frac{0.2 \cdot 360}{10}\right) - Cos\left(\frac{(0.2+0.0000025)\cdot 360}{10}\right)}\right] = 23$$

And thus, to provide the required output frequency resoulution we require 23 fraction bits. To minimise arithmetic overflow errors we included an additional 2 bits in the fraction portion. Bringing the total number of bits required to 30.

A block diagram of the design of the frequency generator is shown in figure 9. In interesting point to note, is that while 30 bits are required internaly for the derivation of the Cosθ output signal. Only the most significant eight fraction bits were provided at the output, as this is all that is required for down stream calculations (and the AtoD). The same situation will apply in a full scale implementation, except in that case around 16 bits will be required at the output.

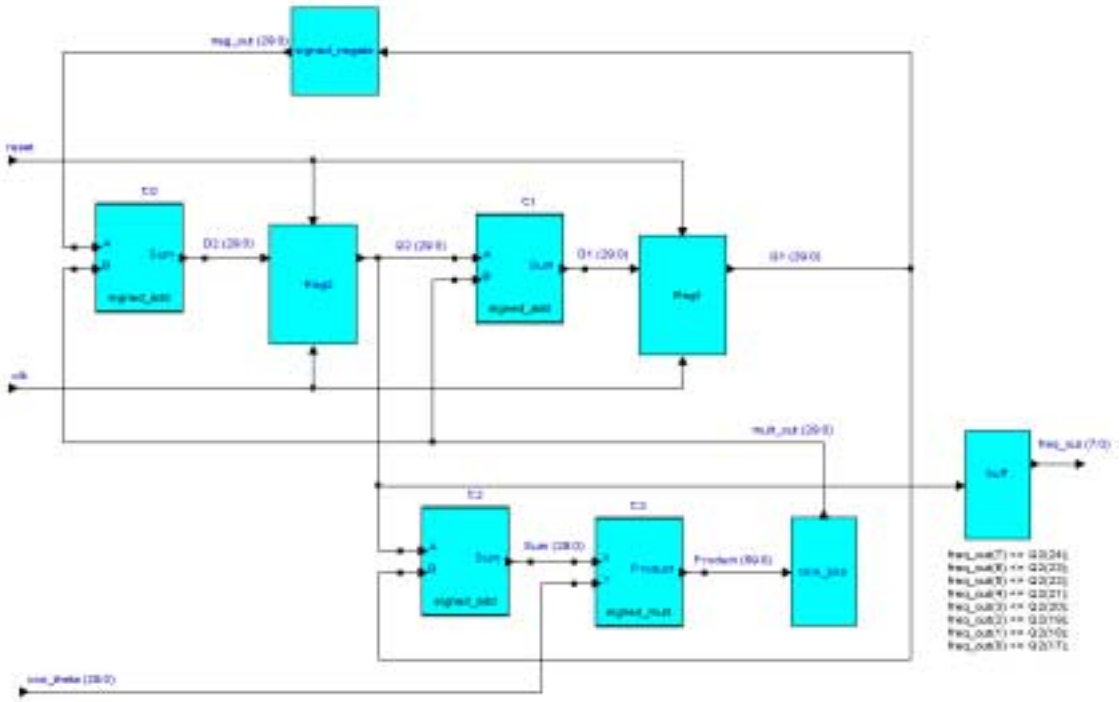


Figure 9, Frequency Generator - Block Diagram

Hardware results

The proof of concept gaussian modulation circuit has been implemented in an Altera Flex 10k20 FPGA using roughly 15,000 gates. The circuit operates correctly producing a series of 290ms modulated gaussian pulses. With the carrier frequency selectable over a range of 200 - 500Hz, by altering the value of the cos_theta input. Figure 10 shows an example of the modulated gaussian pulse, captured via a digital oscilloscope.

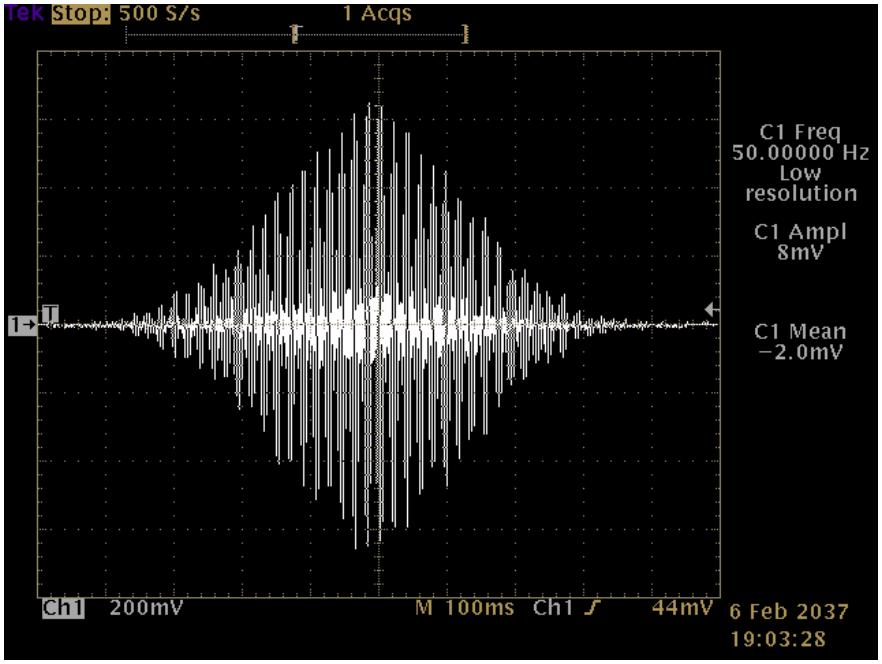


Figure 10, Modulated Gaussian Pulse Output

Matlab investigation FIR vs Polyphase Filter Implementation

We have also modeled the operation of the proposed digital transmitter in Matlab and investigated two potential DSP structures for the implementation of the upsampling (frequency shifting) element. When a digitally represented signal is upsampled (resampled at a higher sample rate) multiple copies of frequency spectra are produced, ranging from the fundamental (original) frequency to fundamental frequency x the upsampling rate (in our case x40). The frequency shift is simply completed by filtering out all the lower spectra copies. Naturally, a digital filter is used. In our first model a 100-tap FIR filter was used. The normalized frequency response of a modulated gaussian pulse after upsampling and FIR filtering is shown in figure 11.

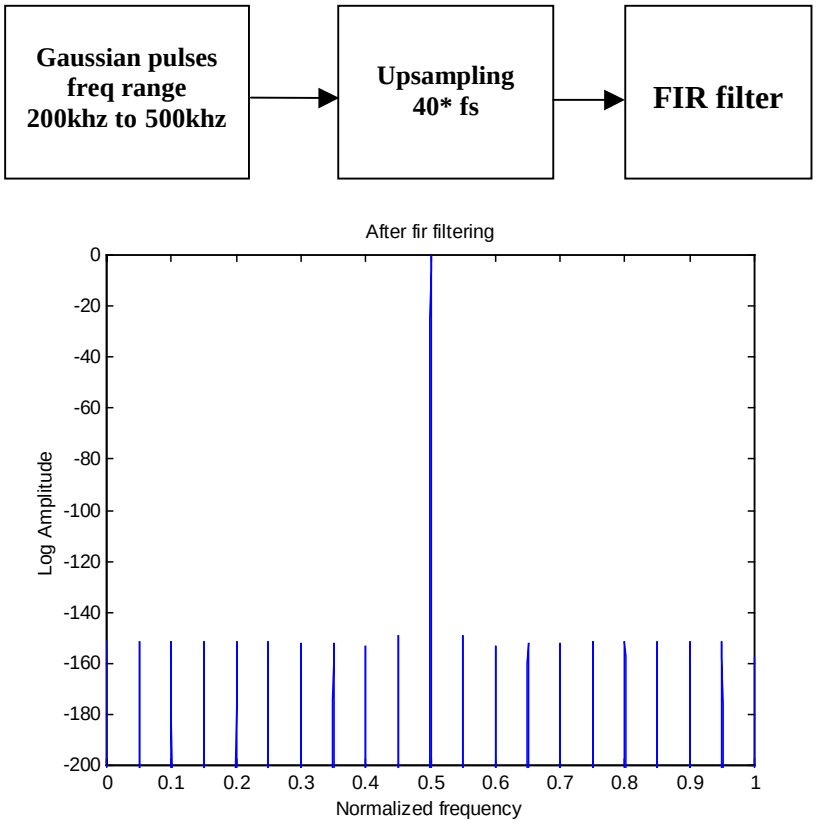


Figure 11, FIR Filer Normalised Frequency Response

An alternative to the FIR filter is the polyphase filter. Its structure enables both upsampling and filtering to be performed in the same process. In our Matlab model we replaced the upsampler and FIR filter with a 100-tap polyphase filter. The normalized frequency response of a modulated gaussian pulse after polyphase filtering is shown in figure 12.

While the structure of a polyphase filter is little more complex than that of the FIR filter it does have a number of properties which make it an attractive proposition for our application.

- The noise floor of the polyphase filter output is lower than that of the FIR filter - this means that it may be possible to implement a lower order (number of taps) polyphase filter compared with an FIR filter producing an equivalent response.

- Only the output section of the polyphase filter runs at the full sample rate - which may simplify the implementation of the input section.
- Upsampling and filtering can be performed in one step - thereby simplifying the design and implementation.
- The polyphase filter can also produce programmable phase delays - making to possible to perform upsampling, filtering and phasing all in the one process.

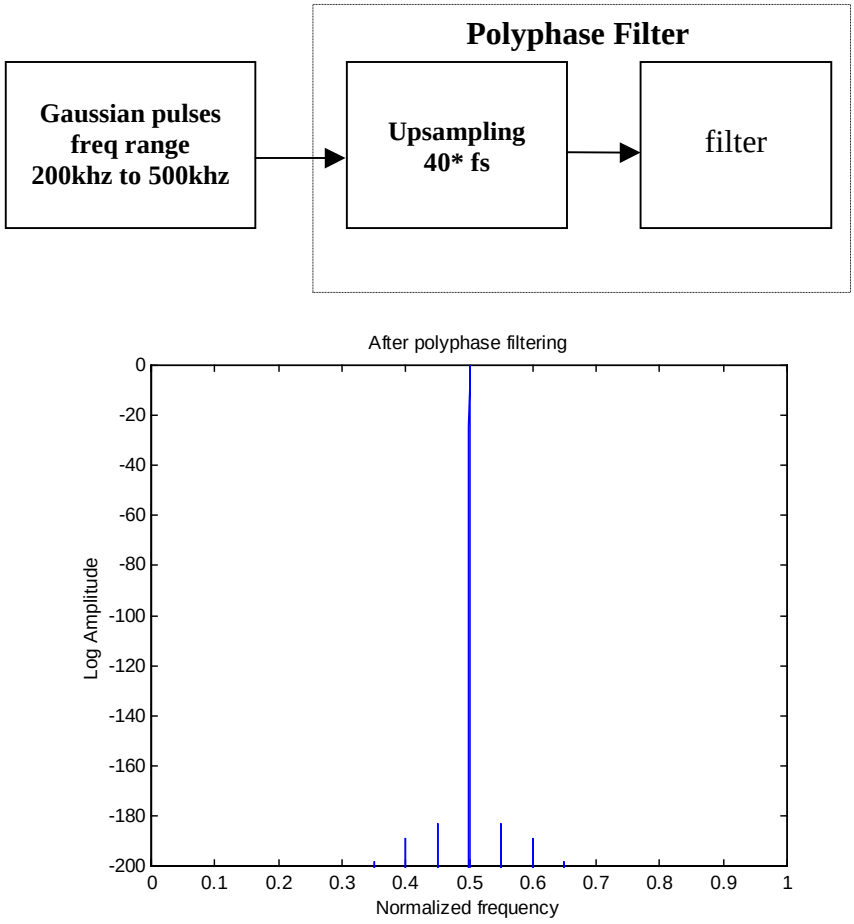


Figure 12, Polyphase Filer Normalised Frequency Response

Discussion

It is our belief that the generation and phasing of transmitter signals for SuperDARN class radars can be readily performed in the digital domain. Furthermore, it should be possible to implement these transmitter functions in today's FPGA technology. While several FPGA devices may be required at present, the continuing rapid advancement of FPGA technology means that within a few years it should be possible to fit the entire transmitter (excluding RF power amplifiers) in one or two large scale devices. The key to the digitization of the SuperDARN radar transmitter circuitry is the utilization and adaptation of the advanced DSP techniques used in modern wireless communication systems. Significant further work is required before the digital design can be finalized, however, we believe that the investigative work presented here demonstrates the concept is sound. While the receiver circuitry is more complex than that of the transmitter, many of the functions are the same or similar.

Therefore, we feel quite confident that the implementation of a digital receiver is quite feasible with technology and resources available to us.

We propose to make the TIGER N.Z. radar a digital evolution of the current analog system. We believe that there are immediate and longer-term benefits to this course of action. Immediate benefits should be a radar hardware that requires less space, and is easier to build and maintain. Pulse shapes and time delays can be readily fixed in the digital domain and digital receivers do not require special tuning. Thus, a digital system should be cheaper to build and maintain while at the same time producing a higher quality result. Longer-term benefits are harder to define, but are most likely to center around the reconfigurable (flexible) nature of the hardware. It would be possible (and most likely common place) to use the same hardware to produce different scan modes, generate arbitrary waveforms etc. An obvious benefit is that we can tailor the system configuration to suit any particular mission - e.g. infinite control over the receiver bandwidth. Another possible benefit could be the 16 (or 20) separate receivers allowing each to be recorded and stored independently - although a draw back would be 16 (20) times the data rate and storage. This would enable post processing beam forming using polyphase filtering to form the beams and interpolate within the beam. There are many other possibilities, the main point is that the hardware of a digital SuperDARN radar can grow and evolve along with the ideas of the community who use it. In the future researchers will be able the change and adjust the radar hardware in the same way that the software is changed and updated today.

Conclusion

In this paper we have presented a proposal for the digital evolution of the TIGER SuperDARN radar. Just as the digitization of consumer products, such as mobile phones, has lead to enhanced features and flexibility, a digital SuperDARN radar will offer improved performance, greater adaptability and new features providing benefits to ionospheric research.

The system we propose here for the next generation TIGER transmitter signal generation chain uses fully digital technology to produce sixteen Gausian shaped, RF, phase referenced pulses, for delivery to a sixteen-antenna array, using only a single clock reference. The system consists of a Gausian pulse generator, a variable RF generator, and a mixer. Multirate filtering will be used to generate phasing and the required 8MHz to 20MHz output frequencies. Different techniques using a variety of DSP structures, including multirate processing and shaping filters, have been investigated for their appropriateness for implementation in FPGA technology. The system offers many cost and manufacturing advantages over current techniques which use a separate frequency synthesiser, delay lines and complex control circuitry to generate the phased pulses for the antenna arrays.

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